	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	11	kajita near yoko.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 17:33	
2	BRS	L2	512	438/243.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 17:42	
3	BRS	L3	3846	(oxidation) near25 (silicon near film)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 17:43	
4	BRS	L4	51	(oxidation) near25 (silicon near film) near25 (fill$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 17:47	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	BRS	L5	70	(oxidation) near25 (silicon near film or soi) near25 (fill$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 17:48	
6	BRS	L6	35	(oxidation) near25 (silicon near film or soi) near25 (fill$3) near25 (substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 17:51	
7	BRS	L7	32	(oxidation) near25 (silicon near film or soi) near25 (buried near oxide) near25 (substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 17:56	
8	BRS	L8	873	(oxidation) near25 (silicon near film or soi) near25 (oxide or box) near25 (substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 18:21	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
9	BRS	L9	433	(oxidation) near25 (sede near wall$1 or sidewall$1) near25 (oxide or box) near25 (substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 18:22	
10	BRS	L10	708	(oxidation) near25 (side near wall$1 or sidewall$1) near25 (oxide or box) near25 (substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/10 18:31	

EAST - [Untitled1:1]

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L7: (749) 6 and (sidewall$1 or (side adj wall$1) or spacer).clm.
L8: (536) 7 and (thermal or oxidation)
L9: (516) 8 and (conduct$3 or metal)
L10: (208) 9 and (expos$3 near (silicon or substrate))
L11: (177) 10 and oxidation
L12: (177) 11 and (insulat$3 or dielectric).clm.
L13: (177) 12 and silicon
L14: (7) 13 and (buried adj oxide)
L15: (176) 13 and (etch$3)
L16: (131) 15 and (etch$3.clm. or thin$3.clm.)
L17: (25) 16 and inner
L18: (1) (6258670).PN.

Search | List | Browse | Queue | Clear

DBs: USPAT; US-PGPUB | Plurals

Default operator: OR | Highlight all hit terms initially

16 and inner

BRS form | IS&R form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	2	3			Im
1			US 20040021160 A1	20040205	94	Semiconductor device, a method of manufacturing the	257/296			Eguchi, Kohei et al.								US 20
2			US 20040016964 A1	20040129	33	Semiconductor device with self-aligned junction contac	257/332	438/589; 438/597		Kim, Ji-Young et al.								US 20
3			US 20030134470 A1	20030717	56	Layer structure having contact hole, fin-shaped cap	438/254	257/E21.038; 257/E21.577;		Ema, Taiji								US 20
4			US 20020185469 A1	20021212	44	Method of micromachining a multi-part cavity	216/41	257/E21.218; 257/E21.235		Podlesnik, Dragan et al.								US 20
5			US 20020001960 A1	20020103	89	Material removal method for forming a structure	438/705	257/E21.011; 257/E21.166;		Wu, Zhiqiang et al.								US 20
6			US 20010038114 A1	20011108	69	Semiconductor integrated circuit device and the metho	257/303	257/E21.019; 257/E21.649		IIjima, Shinpei et al.								US 20
7			US 6664157 B2	20031216	67	Semiconductor integrated circuit device and the metho	438/238	438/240; 438/313		Iijima, Shinpei et al.								US
8			US 6605542 B2	20030812	56	Manufacturing method of semiconductor devices by usi	438/700	257/E21.252; 257/E21.579;		Seta, Shoji et al.								US
9			US 6475838 B1	20021105	9	Methods for forming decoupling capacitors	438/153	257/E29.345; 438/395		Bryant, Andres et al.								US
10			US 6461967 B2	20021008	88	Material removal method for forming a structure	438/705	216/38; 216/87;		Wu, Zhiqiang et al.								US
11			US 6452224 B1	20020917	36	Method for manufacture of improved deep trench eDRAM c	257/296	257/301; 257/303;		Mandelman, Jack A. et al.								US
12			US 6406962 B1	20020618	20	Vertical trench-formed dual-gate FET device structu	438/268	257/E29.137; 257/E29.274;		Agnello, Paul D. et al.								US
13			US 6383921 B1	20020507	5	Self aligned silicide contact method of fabricatio	438/649	438/233; 438/682		Chan, Ching-Hsu et al.								US
14			US 6358782 B1	20020319	36	Method of fabricating a semiconductor device having	438/149	257/E21.703; 257/E27.112;		Masuda, Takashi								US
15			US 6300657 B1	20011009	8	Self-aligned dynamic threshold CMOS device	257/318	257/314; 257/316;		Bryant, Andres et al.								US
16			US 6248622 B1	20010619	10	Fabrication method for ultra short channel device compris	438/239	257/E21.434; 257/E21.507;		Lee, Robin								US
17			US 6159807 A	20001212	8	Self-aligned dynamic threshold CMOS device	438/289	257/E21.415; 257/E29.275;		Bryant, Andres et al.								US
18			US 5960271 A	19990928	10	Short channel self-aligned VMOS field effect transistor	438/197	257/E21.429; 257/E29.13;		Wollesen, Donald L. et al.								US

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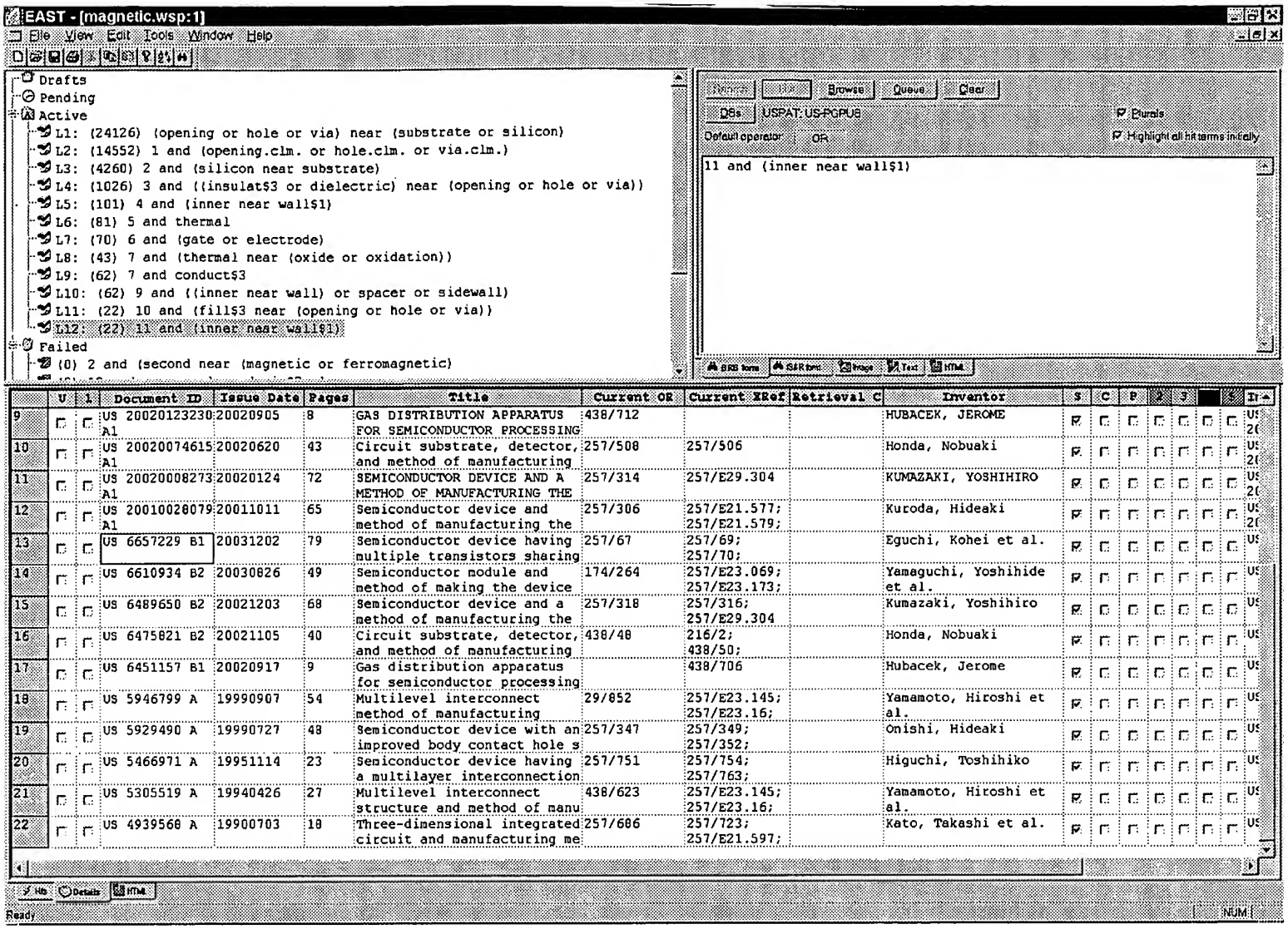

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	2	3		6	Ir
9			US 20020123230 A1	20020905	8	GAS DISTRIBUTION APPARATUS FOR SEMICONDUCTOR PROCESSING	438/712			HUBACEK, JEROME								US 20
10			US 20020074615 A1	20020620	43	Circuit substrate, detector, and method of manufacturing	257/508	257/506		Honda, Nobuaki								US 20
11			US 20020008273 A1	20020124	72	SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE	257/314	257/E29.304		KUMAZAKI, YOSHIHIRO								US 20
12			US 20010026079 A1	20011011	65	Semiconductor device and method of manufacturing the	257/306	257/E21.577; 257/E21.579;		Kuroda, Hideaki								US 20
13			US 6657229 B1	20031202	79	Semiconductor device having multiple transistors sharing	257/67	257/69; 257/70;		Eguchi, Kohei et al.								US
14			US 6610934 B2	20030826	49	Semiconductor module and method of making the device	174/264	257/E23.069; 257/E23.173;		Yamaguchi, Yoshihide et al.								US
15			US 6489650 B2	20021203	68	Semiconductor device and a method of manufacturing the	257/318	257/316; 257/E29.304		Kumazaki, Yoshihiro								US
16			US 6475821 B2	20021105	40	Circuit substrate, detector, and method of manufacturing	438/48	216/2; 438/50;		Honda, Nobuaki								US
17			US 6451157 B1	20020917	9	Gas distribution apparatus for semiconductor processing		438/706		Hubacek, Jerome								US
18			US 5946799 A	19990907	54	Multilevel interconnect method of manufacturing	29/852	257/E23.145; 257/E23.16;		Yamamoto, Hiroshi et al.								US
19			US 5929490 A	19990727	48	Semiconductor device with an improved body contact hole s	257/347	257/349; 257/352;		Onishi, Hideaki								US
20			US 5466971 A	19951114	23	Semiconductor device having a multilayer interconnection	257/751	257/754; 257/763;		Higuchi, Toshihiko								US
21			US 5305519 A	19940426	27	Multilevel interconnect structure and method of manu	438/623	257/E23.145; 257/E23.16;		Yamamoto, Hiroshi et al.								US
22			US 4939568 A	19900703	18	Three-dimensional integrated circuit and manufacturing me	257/686	257/723; 257/E21.597;		Kato, Takashi et al.								US